			Manpower (Man-wks)		
			Senior EE	EE	Designer / tech
1.6.3	FEB	Front End Board:			
1.6.3.1	ASIC	NOvA custom ASIC			
1.6.3.1.1	Prototype I		**4**	**0**	**0**
1.6.3.1.1.1	Administration	Project oversight, collaboration meetings, telecons, reviews, technical and cost reporting	2		0
1.6.3.1.1.2	Documentation	Spec documents, user's manuals, technical reference manuals, test reports			
1.6.3.1.1.3	Design	Design, simulation, layout & verification	2		
1.6.3.1.2	Prototype II		**4**	**0**	**0**
1.6.3.1.2.1	Administration	Project oversight, collaboration meetings, telecons, reviews, technical and cost reporting	2		0
1.6.3.1.2.2	Documentation	Spec documents, user's manuals, technical reference manuals, test reports			
1.6.3.1.2.3	Design	Design, simulation, layout & verification	2		
1.6.3.2	Prototype I	CERN Chip/Ideas ADC evaluation, test and evaluation of NOvA FEB architecture, DSP algorithm testing. USB i/o	**11**	**13**	**12**
1.6.3.2.1	Administration	Project oversight, collaboration meetings, telecons, reviews, technical and cost reporting	4	1	0
1.6.3.2.2	Documentation	Spec documents, user's manuals, technical reference manuals, test reports	3	1	2
1.6.3.2.3	Design	Component evaluation, circuit analysis and simulations, schematic creation, conceptual designs, and pcb CAD layout design	3	4	6
1.6.3.2.4	Assembly	Reflow solder, wire bond, mechanical assembly as necessary			1
1.6.3.2.5	Firmware	Logic conceptual design, VHDL implementation and simulation, download and test		6	
1.6.3.2.6	Software	Software to run test apparatus, data display, and data analysis code			
1.6.3.2.7	Test	Bench top electrical tests, system integration tests.	1	1	3
1.6.3.3	Prototype II	Contains NOvA Front End ASIC and connector to APD module, DSP development, NOvA detector tests, USB i/o	**11**	**13**	**12**
1.6.3.3.1	Administration	Project oversight, collaboration meetings, telecons, reviews, technical and cost reporting	4	1	0
1.6.3.3.2	Documentation	Spec documents, user's manuals, technical reference manuals, test reports	3	1	2
1.6.3.3.3	Design	Component evaluation, circuit analysis and simulations, schematic creation, conceptual designs, and pcb CAD layout design	3	4	6
1.6.3.3.4	Assembly	Reflow solder, wire bond, mechanical assembly as necessary			1
1.6.3.1.5	Firmware	Logic conceptual design, VHDL implementation and simulation, download and test		6	
1.6.3.3.6	Software	Software to run test apparatus, data display, and data analysis code			
1.6.3.3.7	Test	Bench top electrical tests, system integration tests.	1	1	3
1.6.3.4	Prototype III	Contains NOvA Front End ASIC and connector to APD module, DSP development, NOvA detector tests, NOvA specific i/o interface to DAQ combiner	**11**	**13**	**12**
1.6.3.4.1	Administration	Project oversight, collaboration meetings, telecons, reviews, technical and cost reporting	4	1	0
1.6.3.4.2	Documentation	Spec documents, user's manuals, technical reference manuals, test reports	3	1	2
1.6.3.4.3	Design	Component evaluation, circuit analysis and simulations, schematic creation, conceptual designs, and pcb CAD layout design	3	4	6
1.6.3.4.4	Assembly	Reflow solder, wire bond, mechanical assembly as necessary			1
1.6.3.1.5	Firmware	Logic conceptual design, VHDL implementation and simulation, download and test		6	
1.6.3.4.6	Software	Software to run test apparatus, data display, and data analysis code			
1.6.3.4.7	Test	Bench top electrical tests, system integration tests.	1	1	3
1.6.3.5	Prototype IV	Pre-production FEB	**11**	**13**	**12**
1.6.3.5.1	Administration	Project oversight, collaboration meetings, telecons, reviews, technical and cost reporting	4	1	0
1.6.3.5.2	Documentation	Spec documents, user's manuals, technical reference manuals, test reports	3	1	2
1.6.3.5.3	Design	Component evaluation, circuit analysis and simulations, schematic creation, conceptual designs, and pcb CAD layout design	3	4	6
1.6.3.5.4	Assembly	Reflow solder, wire bond, mechanical assembly as necessary			1
1.6.3.1.5	Firmware	Logic conceptual design, VHDL implementation and simulation, download and test		6	
1.6.3.5.6	Software	Software to run test apparatus, data display, and data analysis code			
1.6.3.5.7	Test	Bench top electrical tests, system integration tests.	1	1	3
			52	**52**	**48**